WHAT IS CLAIMED IS:

1. A Dynamic Random Access Memory (DRAM) , comprising:

a plurality of strip-type active areas on a substrate;

a plurality of shallow trench isolation regions on the substrate for isolating each of the active areas;

a plurality of word lines above the active areas and the shallow trench isolation regions, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein every two of the first overlapping portions are separated by every two of the second overlapping portions on each of the active areas and each of the first overlapping portions is next to each of the second overlapping portions on every two neighboring active areas; and

a capacitor array in the active areas, each of the capacitors being in each of the first overlapping portions, the capacitor including a deep trench structure and a collar isolation, wherein a memory cell is formed by the word line in one of the second overlapping portions and the capacitor in one of the first overlapping portions.

2. The DRAM as recited in claim 1, wherein the deep trench structure of the capacitor comprises:

a bottom plate on an interface region of the substrate and a lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate; and

a top plate, formed by filling the deep trench structure and covering the

dielectric layer with a conductive material.

3. The DRAM as recited in claim 2, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

4. The DRAM as recited in claim 2, wherein the dielectric layer is a composite layer comprising silicon nitride and silicon oxide.

5. The DRAM as recited in claim 2, wherein the top plate comprises a polysilicon layer doped with arsenic.

6. The DRAM as recited in claim 2, wherein the collar isolation of the capacitor comprises a collar oxide layer on an upper sidewall portion of the deep trench structure and above the dielectric layer, wherein the collar oxide layer further comprises a first collar portion and a second collar portion, the first collar portion being on an adjacent portion of two of the neighboring capacitors, the second collar portion being on a non-adjacent portion of two of the neighboring capacitors, the first collar portion being longer than the second collar portion in a depth direction of the deep trench and a depth of the second collar portion being the same as a depth of the top plate.

7. The DRAM as recited in claim 6, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å for respectively isolating the

neighboring capacitors and sufficiently decreasing a leakage current of the substrate theresurrounding.

8. The DRAM as recited in claim 6, wherein the capacitor further comprises:

a buried strap conductive layer, above the second collar portion, including a diffusion conductive region in the substrate outside the buried strap conductive layer; and

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in a word line direction.

9. The DRAM as recited in claim 8, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

10. The DRAM as recited in claim 8, wherein the trench top isolation further comprises a silicon oxide layer.

11. The DRAM as recited in claim 1, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

12. The DRAM as recited in claim 1, further comprising a gate oxide layer between the substrate and the word lines.

13. The DRAM as recited in claim 1, wherein the word line further comprises a doped silicon layer and a silicon tungsten layer as a gate electrode.

14. The DRAM as recited in claim 8, wherein two sides of each of the second overlapping portion further comprise a source and a drain of each of the memory cell.

15. A Dynamic Random Access Memory (DRAM) , comprising:

a plurality of strip-type active areas on a substrate;

a plurality of shallow trench isolation regions on the substrate for isolating each of the active areas;

a plurality of word lines above the active areas and the shallow trench isolation regions, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein every two the first overlapping portions is separated by every two the second overlapping portions on each of the active areas, and each of the first overlapping portions is next to each of the second overlapping portions on every two the neighboring active areas; and

a capacitor array on the active areas, each of the capacitors being on each of the first overlapping portions, the capacitor comprising:

a deep trench structure, comprising an upper sidewall region and a lower sidewall region;

a collar oxide layer, on an upper sidewall portion of the deep trench structure, comprising a first collar portion and a second collar portion, the first collar portion being on an adjacent portion of two of the neighboring capacitors,

the second collar portion being on a non-adjacent portion of two of the neighboring capacitors, the first collar portion being longer than the second collar portion in a depth direction of the deep trench structure, the first collar portion being used to isolate the neighboring capacitors and the second collar portion being used to reduce sufficiently a leakage current of the substrate surrounding thereof;

a buried strap conductive layer, above the second collar portion, including a diffusion conductive region in the substrate outside the buried strap conductive layer; and

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in the word line direction;

wherein a memory cell formed by the word line in one of the second overlapping portions controls the capacitor via the diffusion conductive region in one of the first overlapping portions.

16. The DRAM as recited in claim 15, wherein the deep trench structure of the capacitor comprises:

a bottom plate on an interface region of the substrate and the lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate; and

a top plate, formed by filling the deep trench structure and covering the dielectric layer with a conductive material.

17. The DRAM as recited in claim 16, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

18. The DRAM as recited in claim 16, wherein the dielectric layer is a composite layer comprising silicon nitride and silicon oxide.

19. The DRAM as recited in claim 16, wherein the top plate comprises a polysilicon layer doped with arsenic.

20. The DRAM as recited in claim 15, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å.

21. The DRAM as recited in claim 15, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

22. The DRAM as recited in claim 15, wherein the trench top isolation further comprises a silicon oxide layer.

23. The DRAM as recited in claim 15, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

24. The DRAM as recited in claim 15, further comprising a gate oxide layer

between the substrate and the word lines.

25. The DRAM as recited in claim 15, wherein the word line further comprises a doped silicon layer and a silicon tungsten layer as a gate electrode.

26. The DRAM as recited in claim 15, wherein two sides of each of the second overlapping portion further comprise a source and a drain of each memory cell.

27. A method of fabricating a Dynamic Random Access Memory (DRAM), the DRAM having a substrate comprising a pad oxide layer and a silicon nitride layer formed in turn thereon and an capacitor array, each capacitor having a deep trench structure therein, every two capacitors being a capacitor subassembly, the capacitor subassemblies in a row of the capacitor array not neighboring with each other, and the capacitor subassemblies in neighboring rows of the capacitor array not neighboring with each other, the method comprising:

in each capacitor,

forming a collar oxide layer on an upper sidewall region of the deep trench structure;

forming a bottom plate on an interface region of the substrate and a lower sidewall portion of the deep trench structure;

forming a dielectric layer on an internal surface of the bottom plate in the deep trench structure by using the collar oxide as a mask;

forming a top plate in the deep trench structure to cover the dielectric layer;

removing part of the collar oxide layer to form a first collar portion and a

second collar portion, wherein the first collar portion is an adjacent portion of the collar oxide layer in the two capacitors of the capacitor subassembly, the second collar portion is a non-adjacent portion of the collar oxide layer in the two capacitors of the capacitor subassembly, the first collar portion being longer than the second collar portion in depth direction of the deep trench structure, the first collar portion being used to isolate the neighboring capacitors and the second collar portion being used to sufficiently reduce a leakage current of the substrate theresurrounding; and

forming a buried strap conductive layer above the second collar portion and the top plate; and

on the substrate,

forming a plurality of strip-type active areas and a plurality of shallow trench isolation regions in turn thereon;

forming a gate oxide layer thereon;

forming a plurality of word lines on the columns of the capacitor array, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein each the first overlapping portion therein comprises each capacitor subassembly; and

forming a plurality of sources and drains on two sides of each the second overlapping portion, wherein a memory cell is formed by the word line on one of the second overlapping portions controlling the capacitor via the diffusion conductive region on one of the first overlapping portions.

28. The method of fabricating a DRAM as recited in claim 27, wherein

forming the collar oxide layer comprises:

depositing a collar nitride layer to cover the substrate;

depositing a sacrificial photoresist to cover the collar nitride layer;

etching part of the sacrificial photoresist and leaving a lower portion of the sacrificial photoresist;

etching part of the collar nitride layer by utilizing the lower portion of the sacrificial photoresist as a mask;

removing the lower portion of the sacrificial photoresist and leaving a lower portion of the collar nitride layer;

forming the collar oxide layer on the upper sidewall region of the deep trench structure to a thickness of about 400 Å-500Å by a thermal process; and

removing the lower portion of the collar nitride layer.

29. The method of fabricating a DRAM as recited in claim 27, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

30. The method of fabricating a DRAM as recited in claim 27, wherein the dielectric layer is formed by first depositing a silicon nitride layer on the lower sidewall portion of the deep trench structure and then heating to form a composite layer comprising silicon nitride and silicon oxide.

31. The method of fabricating a DRAM as recited in claim 27, wherein the top plate is formed by forming a doped polysilicon layer comprising arsenic.

32. The method of fabricating a DRAM as recited in claim 27, wherein removing part of the collar oxide layer to form the first collar portion and the second collar portion comprises:

forming a photoresist for covering the silicon nitride layer, a first portion of the collar oxide and part of the top plate of each capacitor subassembly to expose a second portion of the collar oxide; and

etching the second portion of the collar oxide to a top surface of the top plate by using the photoresist as a mask to form the first collar portion and the second collar portion.

33. The method of fabricating a DRAM as recited in claim 27, wherein forming the buried strap conductive layer comprises:

forming a silicon layer on the top surface of the top plate and the second collar portion in the deep trench structure;

etching part of the silicon layer to a depth;

performing an ion implant process to dope the silicon layer; and

performing a thermal process to form a diffusion conductive region.

34. The method of fabricating a DRAM as recited in claim 27, wherein forming the active areas with a strip-type and the shallow trench isolation regions comprising:

forming a plurality of photoresist strips for covering the capacitors on each row of the capacitor array;

etching the substrate to an upper edge of the second collar portion to form the shallow trench isolation regions;

depositing an oxide layer on the substrate to cover the shallow trench isolation regions; and

utilizing a chemical mechanical polishing process to planarize the substrate having the active areas.

35. The method of fabricating a DRAM as recited in claim 27, wherein forming the word lines comprises:

depositing a polysilicon layer on the gate oxide layer;

doping the polysilicon layer to decrease the resistance sufficiently;

depositing a silicide layer on the polysilicon layer; and

patterning the silicide layer and the polysilicon layer to form the word lines.